IN THE SPECIFICATION

Please amend the specification as follows:

Please replace paragraph **[009]** with the following rewritten paragraph:

- - Typically, at present the splitter 204, FIG, 2, is usually implemented as a passive splitter utilizing passive elements such as [[a]] numerous ~~resistor~~ resistors or a set of transformers. As an example, the splitter 204 may be implemented utilizing a Wilkinson divider or cascaded passive network of Wilkinson type. Unfortunately, the use of a passive splitter degrades the overall performance of the tuners 206, 208, 210 and 212 because the passive splitters will cause insertion losses of between approximately 3 to 6 decibels ("dB") per split, which degrades the performance of the associated tuners by ~~effecting~~ affecting the overall noise figure and signal-to-noise ratio ("SNR") of the system 200. - -

Please replace paragraph **[015]** with the following rewritten paragraph:

- - An active splitter is disclosed for splitting ~~and~~ an input signal into a plurality of split output signals. The active splitter may include a plurality of active circuits connected in parallel that produce the plurality of split output signals from the received input signal, where each active circuit of the plurality of active circuits produces a corresponding split output signal from the plurality of split output signals that is substantially similar to the received input signal. - -

Please replace paragraph **[036]** with the following rewritten paragraph:

- - The Active Splitter 500 may also be dynamic or programmable with the assistance of a controller 536 that may be any microcontroller or microprocessor capable of either being

hardwired or running software (not shown) that may be resident on the microprocessor, the Active Splitter 500 or a device external to the Active Splitter ~~600~~ 500. In an example implementation of an Active Splitter 500 with a controller 536, the Active Splitter ~~600~~ 500 may have circuitry (not shown) capable of determining the output values of the four signal splitting stage active circuits 510, 512, 514 and 516. If the LNA 508 is implemented as a variable gain amplifier LNA ("VGA-LNA"), the controller 536 could then adjust the amount of gain produced by the VGA-LNA 508 by sending control signals via signal path 538. The controller 536 could then adjust the gain produced by the VGA-LNA 508 in response to the outputs of the four signal splitting stage active circuits 510, 512, 514 and 516 being below a certain predetermined signal strength. - -

Please replace paragraph **[047]** with the following rewritten paragraph:

- - As an example, the common-emitter amplifier 708 may include ~~an~~ a Darlington pair transistor 716, a base 718, collector 720, emitter 722 and collector resistor 724. It is appreciated by those skilled in the art that there are a number of potential circuit topologies that may be utilized to implement the common-emitter amplifier 708. Additionally, while the amplifiers shown are single ended amplifiers, it is appreciated by those skilled in the art that differential amplifiers may also be utilized without limitation or departing from the spirit of the invention. - -

Please replace paragraph **[051]** with the following rewritten paragraph:

- - Again, it is appreciated by those skilled in the art that the first gain stage 704 may also be implemented utilizing a voltage follower instead of the common-emitter amplifier 708 shown in the first gain stage 704 without limitation or departing from the spirit of the invention. In the

case of a situation where the Active Splitter 700 will operate in an environment that has linearity requirements that are stringent, [[a]] an emitter follower may be utilized instead of the common emitter amplifier 708. - -

Please replace paragraph **[069]** with the following rewritten paragraph:

- - It is appreciated that by those skilled in the art that active switch 1000 described in FIG. 10 may be implemented within a DBS multi-switch system and the control signals communicated via signal path 1098 (which may be implemented as a standard communication bus) may utilize, for example, a communication protocol such as the Digital Satellite Equipment Control System known as "DiSEqC™." DiSEqC™ is a well-known protocol that communicates on a communication bus between satellite receivers and peripheral equipment using only an existing coaxial cable. DiSEqC™ is a protocol that ~~allow~~ allows satellite receivers to both switch between multiple low-noise block downconverters ("LNBs") connected to the satellite receiver, via a coaxial cable, and change an LNB's individual polarization state. - -

Please replace paragraph **[070]** with the following rewritten paragraph:

- - FIG. 11 is a flow-chart diagram 1100 showing the process performed by the Active Splitters shown in both FIG. 6 and FIG. 7. The process starts at step 1102, when the first gain stage 604 amplifies the received input signal 602 to the Active Splitter 600 in step 1104. The Active Splitter 600 then drives a plurality of emitter followers 610, 612 and 614 within the second stage 606 with the output 662 from the first stage in step 1106. In response the emitter followers 610, 612 and 614 produce their respective outputs 670, 672 and 674 and the process ends in step 1110. However, if the Active Splitter 600 has the optional controller 676, the

process may continue to optional determination step 1108 where the controller 676 determines whether the outputs 670, 672 and 674 of the plurality of the emitter followers 610, 612 and 614 are within a predetermined range. If the values of the outputs 670, 672 and 674 are within the predetermined range, the controller 676 allows the Active Splitter 600 to continue to operate without any modification and the process ends in step 1110. - -

Please replace paragraph **[072]** with the following rewritten paragraph:

- - If instead the values of the outputs 670, 672 and 674 are not within the predetermined range, the controller 676 then again sends a control signal to the first gain stage 604 to adjust the gain of the first stage in step ~~909~~ 1109 and the process continues in the same fashion until it ends in step 1110. - -

Please replace paragraph **[075]** with the following rewritten paragraph:

- - If instead the values of the outputs 870, 872 and 874 are not within the predetermined range, the controller 876 then again sends a control signal to the first gain stage 804 to adjust the gain of the first stage in step ~~1009~~ 1209 and the process continues in the same fashion until it ends in step 1210. - -